Part of Paper #9

TOWNSEND AND TOWNSEND AND CREW LLP
DANIEL J. FURNISS (State Bar No. 73531)
THEODORE G. BROWN, III (State Bar No. 114672)
JORDAN TRENT JONES (State Bar No. 16660)
379 Lytton Avenue
Palo Alto, California 94301
Telephone: (650) 326-2400
Facsimile: (650) 326-2422

O'MELVENY & MEYERS LLP
PATRICK LYNCH (State Bar No. 39749)
KENNETH R. O'ROURKE (State Bar No. 120144)
400 South Hope Street
Los Angeles, California 90071-2899
Telephone: (213) 430-6000
Facsimile: (213) 430-6407

THELEN REID & PRIEST LLP
KENNETH L.NISSLY (State Bar No. 77589)
SUSAN G. van KEULEN (State Bar No. 136060)
333 West San Carlos Street, 17th Floor
San Jose, California 95110-2701
Telephone: (408) 292-5800
Facsimile: (408) 287-8040

Attorneys for
HYNIX SEMICONDUCTOR INC.,
HYNIX SEMICONDUCTOR AMERICA, INC.,
HYNIX SEMICONDUCTOR U.K. LTD., and
HYNIX SEMICONDUCTOR DEUTSCHLAND GmbH

UNITED STATES DISTRICT COURT

FOR THE NORTHERN DISTRICT OF CALIFORNIA

SAN JOSE DIVISION

HYNIX SEMICONDUCTOR INC., HYNIX SEMICONDUCTOR AMERICA, INC., HYNIX SEMICONDUCTOR U.K. LTD. and HYNIX SEMICONDUCTOR DEUTSCHLAND GmbH, Plaintiffs, v. RAMBUS, INC.,	Case No. CV 00-20905 RMW **HYNIX' PRELIMINARY INVALIDITY CONTENTIONS**

Defendant.

RAMBUS, INC.,

Counterclaimant,

v.

HYNIX SEMICONDUCTOR INC., HYNIX SEMICONDUCTOR AMERICA, INC., HYNIX SEMICONDUCTOR U.K. LTD. and HYNIX SEMICONDUCTOR DEUTSCHLAND GmbH,

Counterdefendants.

Pursuant to Rules 3-3 and 3-4 of the Patent Local Rules, Plaintiffs Hynix Semiconductor Inc., Hynix Semiconductor America Inc., Hynix Semiconductor U.K. LTD., and Hynix Semiconductor Deutschland GmbH (collectively "Hynix") hereby make their Preliminary Invalidity Contentions in response to Defendant Rambus, Inc.'s ("Rambus") Disclosure of Asserted Claims. Hynix has presented its invalidity contentions basued upon Rambus' apparent claim interpretations and the claim construction Hynix will present to the Court.

These contentions are made without prejudice to Hynix' right to obtain and present at trial or in pretrial proceedings such additional information as may be acquired through discovery or otherwise in this action. Specifically, Hynix bases its present invalidity contentions on Rambus' Preliminary Infringement Contentions and Disclosure of Asserted Claims. If the Court permits Rambus, on motion to, assert different representative claims, Hynix reserves the right to supplement its invalidity contentions. Formal discovery is on-going and Hynix' investigation is still underway. Moreover, the scope of prior art relevant in this case may be further altered or defined by the Court's ruling on claim construction. Hynix, therefore, reserves the right to modify or add to this list as provided under the Patent Local Rules.

I. ASSERTED CLAIMS

Rambus' Disclosure of Asserted Claims identified the following claims from nine of the eleven patents-in-suit.[1]

U.S. Patent Number	Asserted Claims
5,915,105 ("the '105 patent")	31, 34, 35, 40
5,953,263 ("the '263 patent")	1, 2, 3, 4
5,995,443 ("the '443 patent")	1, 3, 6
6,032,214 ("the '214 patent")	15, 18, 25, 26
6,034,918 ("the '918 patent")	18, 24, 33
6,035,365 ("the '365 patent")	1, 4
6,038,195 ("the '195 patent")	11, 17, 18, 19
6,067,592 ("the '592 patent")	35, 38
6,101,152 ("the '152 patent")	12, 14, 16

---

[1] Rambus' Disclosure Of Asserted Claims did not identify any representative claims from the '215 or '804 patents. By letter of counsel, Rambus later attempted to cure this omission by informally identifying claim 4 of the '365 patent and claim 3 of the '265 patent as representative of the '804 patent and claims 1, 3 and 6 of the '443 patent as representative of the '215 patent.

Rambus' Disclosure Of Asserted Claims also listed claims from a pending Rambus patent application that has not issued as a patent. On September 21, 2001, Rambus informally notified Hynix of its intention to substitute claims from two additional pending patent applications for asserted claims of the '105, '214 and '263 patents. Since these applications have yet to issue as patents and are not included in Rambus' counterclaim, the applications have no legal significance within this litigation. *See GAF Building Materials Corp. v. Elk Corp. of Dallas*, 90 F.3d 479, 483 (Fed. Cir. 1996); 35 U.S.C. § 154(a)(2); 35 U.S.C. § 271(a)] Accordingly, Hynix is not making any contentions regarding such claims at this time.

Hynix is only making invalidity contentions for the representation claims originally disclosed in Rambus' Disclosure of Asserted Claims. Hynix, however, reserves the right to amend or supplement its Preliminary Invalidity Contentions as permitted on motion to the Court.

II. PRIOR ART REFERENCES—Patent Local Rule 3-3(a)

Pursuant to Patent Local Rule 3-3(a), Exhibit A identifies the prior art references in support of Hynix' Preliminary Invalidity Contentions.

///

///

///

III. ANTICIPATION OR OBVIOUSNESS—Patent Local Rule 3-3(b)

Pursuant to Patent Local Rule 3-3(b), Hynix identifies the following prior art references in support of its preliminary invalidity contentions. Where anticipation is indicated, reference is made to individual prior art references. For obviousness, Hynix has listed combinations of references. The motivation to combine references for obviousness are set forth in the invalidity claim charts. To the extent that any references are not held to be anticipatory, Hynix contends that the representative claims are obvious in view of such references.

1. The '105 Patent Invalidity Contentions

Claims	Anticipated By References	Obvious In View Of Reference Combinations
31	* Gigabit Logic * Redwine * Aichelmann * Tam * Yoshimoto * Fischer * SCI 1 * Bajwa * Siemens PIP * Ono * Pelgrom (9/86) * Pelgrom (6/87) * Higuchi * Ohno	
34[31]	* SCI 1 * Siemens PIP * Pelgrom (9/86) * Pelgrom (6/87)	* Gigabit Logic in combination with any of the following: Wiggers; Grover; Lofgren; Flora; OR Uvieghara. * Redwine in combination with any of the following: Wiggers; Grover; Lofgren; Flora; OR Uvieghara. * Aichelmann in combination with any of the following: Wiggers; Grover; Lofgren; Flora; OR

1. The '105 Patent Invalidity C ntentions		
		Uvieghara. Tam in combination with any of the following: Wiggers; Grover; Lofgren; Flora; OR; Uvieghara. * Yoshimoto in combination with any of the following: Wiggers; Grover; Lofgren; Flora; OR Uvieghara. * Ono OR Higuchi OR Ohno in combination with any of the following: Wiggers; Grover; Lofgren; Flora; OR Uvieghara * Fischer in combination with any of the following: Wiggers; Grover; Lofgren; Flora; OR Uvieghara.
35[34]	* Higuchi * SCI 1	* Gigabit Logic in combination with any of the following: Wiggers; Grover; Lofgren; Flora; OR Uvieghara. * Redwine in combination with any of the following: Wiggers; Grover; Lofgren; Flora; OR Uvieghara. * Aichelmann in combination with any of the following: Wiggers; Grover; Lofgren; Flora; OR Uvieghara. * Tam in combination with any of the following: Wiggers; Grover; Lofgren; Flora; OR Uvieghara. * Yoshimoto in combination with any of the following: Wiggers; Grover; Lofgren; Flora; OR Uvieghara. * Fischer AND Redwine in combination with any of the following: Wiggers; Grover; Lofgren; Flora; OR Uvieghara. * SCI 1 in combination with any of the following: Gigabit Logic; Redwine; Aichelmann; Tam; Yoshimoto; OR Higuchi. * Siemens PIP in combination with any of the following: Gigabit Logic; Redwine; Aichelmann; Tam; Yoshimoto; OR Higuchi.
40[36]	* SCI 1	* Gigabit Logic in combination with any of the following: Wiggers; Grover; Lofgren; Flora; OR Uvieghara. * Yoshimoto in combination with any of the following: Wiggers; Grover; Lofgren; Flora; OR

1. The '105 Patent Invalidity Contentions		
		Uvieghara. * Fischer in combination with any of the following: Wiggers; Grover; Lofgren; Flora; OR Uvieghara. * Siemens PIP in combination with any of the following: Gigabit Logic; Redwine; Aichelmann; Tam; Yoshimoto; OR Higuchi. * Ono or Ohno in combination with any of the following: Wiggers; Grover; Lofgren; Flora; OR Uvieghara.

2. The '263 Patent Invalidity Contentions		
Claims	**Anticipated By References**	**Obvious In View Of Reference Combinations**
1	* Yamaguchi * Saccardi * Kumagai * Fischer * Siemens PIP * Kanopoulos * Miller * Pelgrom (9/86) * Pelgrom (6/87) * SCI 1	* Fischer in combination with any of the following: Rau; Kawamasa; Hasegawa; Saccardi; OR Kumagai. * Ohno in combination with any of the following: Rau; Kawamasa; Hasegawa; Saccardi; Kumagai; OR Bajwa. * SCI 1 in combination with any of the following: Rau; Kawamasa; Hasegawa; Saccardi; OR Kumagai.
2[1]	* Yamaguchi * Saccardi * Kumagai * Siemens PIP * Kanopoulos * Miller * Ohno * SCI 1	* Pelgrom (9/86) OR Pelgrom (6/87) with Yamaguchi * Fischer in combination with any of the following: Rau; Kawamasa; Hasegawa; Saccardi; OR Kumagai. * SCI 1 in combination with any of the following: Rau; Kawamasa; Hasegawa; Saccardi; OR Kumagai.
3[2]	* Yamaguchi * Saccardi * Kumagai	* Fischer in combination with any of the following: Rau; Kawamasa; Hasegawa; Saccardi; OR Kumagai. * SCI 1 in combination with any of the following:

2. The '263 Patent Invalidity Contentions		
	* Fischer * Siemens PIP * Kanopoulos * Miller * Pelgrom (9/86) * Pelgrom (6/87) * Ohno * SCI 1	Rau; Kawamasa; Hasegawa; Saccardi; OR Kumagai.
4[1]	* Yamaguchi * Saccardi * Kumagai * Fischer * Siemens PIP * Kanopoulos * Miller * Pelgrom (9/86) *Pelgrom (6/87) * SCI 1	* Fischer in combination with any of the following: Rau; Kawamasa; Hasegawa; Saccardi; OR Kumagai. * SCI 1 in combination with any of the following: Rau; Kawamasa; Hasegawa; Saccardi; OR Kumagai.

3. The '443 Patent Invalidity Contentions		
Claims	**Anticipated By References**	**Obvious In View Of Reference Combinations**
1	* Watanabe * Ohta * SCI 1	* Fischer in combination with any of the following: Watanabe; Yamaguchi; Redwine; OR Novak. * Siemens PIP in combination with any of the following: Watanabe; Yamaguchi; Redwine; OR Novak.
3[1]	* SCI 1	* Watanabe in combination with any of the following: Wiggers; Grover; Lofgren; Flora; OR Uvieghara. * Ohta in combination with any of the following: Wiggers; Grover; Lofgren; Flora; OR Uvieghara.

3. The '443 Patent Invalidity Contentions		
		* Fischer in combination with any of the following: Watanabe; Yamaguchi; Redwine; OR Novak, AND in combination with any of the following: Wiggers; Grover; Lofgren; Flora; OR; Uvieghara; OR Flora * Siemens PIP in combination with any of the following: Watanabe; Yamaguchi; Redwine; OR Novak.
6[1]		* Fischer in combination with any of the following: Rau; Kawamasa; Hasegawa; Saccardi; OR Kumagai. * SCI 1 in combination with any of the following: Rau; Kawamasa; Hasegawa; Saccardi; OR Kumagai. * Siemens PIP in combination with any of the following: Watanabe; Yamaguchi; Redwine; OR Novak.

4. The '214 Patent Invalidity Contentions		
Claims	**Anticipated By References**	**Obvious In View Of Reference Combinations**
15	* Yamaguchi * Fischer * SCI 1 * Siemens PIP * Miller * Pelgrom (9/86) * Pelgrom (6/87)	
18[15]	* Fischer * Siemens PIP * Miller *Pelgrom (9/86) *Pelgrom (6/87) * SCI 1	* Fischer in combination with any of the following: Rau; Kawamasa; Hasegawa; Saccardi; OR Kumagai. * SCI 1 in combination with any of the following: Rau; Kawamasa; Hasegawa; Saccardi; OR Kumagai.

4. The '214 Patent Invalidity Contentions		
25[15]	* Fischer *Pelgrom (9/86) * SCI 1 * Pelgom (6/87) * Siemens PIP	
26[25]	* SCI 1 * Pelgrom (9/86) * Siemens PIP * Pelgrom (6/87)	* Fischer in combination with any of the following: Wiggers; Grover; Lofgren; Flora; OR Uvieghara.

5. The '918 Patent Invalidity Contentions		
Claims	**Anticipated By References**	**Obvious In View Of Reference Combinations**
18	* Fischer * SCI 1 * Pelgrom (6/87) * Siemens PIP * Kanopoulos * Taguchi * Miller * Pelgrom (9/86)	
24[18]	* Fischer * Siemens PIP * Kanopoulos * Miller * Pelgrom (9/86) * Pelgrom (6/87) * SCI 1	* Fischer in combination with any of the following: Rau; Kawamasa; Hasegawa; Saccardi; OR Kumagai. * Taguchi with any of the following: Rau, Kawamasa, Hasegawa, Hasegawa, Saccardi, Kumagai, OR Bajwa * SCI 1 in combination with any of the following: Rau; Kawamasa; Hasegawa; Saccardi; OR Kumagai.
33[18]	* Siemens PIP	* Fischer in combination with any of the following:

5. The '918 Patent Invalidity Contenti ns		
	* Pelgrom (9/86) * Pelgrom (6/87) * SCI 1	Wiggers; Grover; Lofgren; Flora; OR Uvieghara. SCI 1 in combination with any of the following: Kawamasa; Hasegawa; Saccardi; OR Kumagai. Kanopoulos or Taguchi or Miller in combination with any of the following: Wiggers; Grover; Lofgren; Flora; OR Uvieghara.

6. The '365 Patent Invalidity Contentions		
Claims	**Anticipated By References**	**Obvious In View Of Reference Combinations**
1	* Fischer * Siemens PIP * Kanopoulos * Miller * Pelgrom (9/86) * Pelgrom (6/87) *SCI 1	* Fischer in combination with any of the following: Rau; Kawamasa; Hasegawa; Saccardi; OR Kumagai. * SCI 1 in combination with any of the following: Rau; Kawamasa; Hasegawa; Saccardi; OR Kumagai. * Ohno with Rau; Kawamasa; Hasegawa; Saccardi; Kumagai; OR Bajwa.
4[1]	* Siemens PIP * Pelgrom (9/86) * Pelgrom (6/87) * SCI 1	* Fischer in combination any of the following: Rau; Kawamasa; Hasegawa; Saccardi; OR Kumagai. * Fischer in combination any of the following: Rau; Kawamasa; Hasegawa; Saccardi; OR Kumagai, AND in combination with any of the following: Wiggers; Grover; Lofgren; Flora; OR Uvieghara. * SCI 1 in combination with any of the following: Rau; Kawamasa; Hasegawa; Saccardi; OR Kumagai. * Kanopoulos or Miller or Ohno in combination with any of the following: Wiggers; Grover; Lofgren; Flora; OR Uvieghara.

7. The '195 Patent Invalidity Contentions

7. The '195 Patent Invalidity Contentions		
Claims	**Anticipated By References**	**Obvious In View Of Reference Combinations**
11	* Saccardi * Yamaguchi * Kumagai * Fischer * Siemens PIP * Kanopoulos * Miller * Pelgrom (9/86) * Pelgrom (6/87) * SCI 1	* Fischer in combination with any of the following: Rau; Kawamasa; Hasegawa; Saccardi; OR Kumagai. * Ohno in combination with any of the following: Rau; Kawamasa; Hasegawa; Saccardi; Kumagai; OR Bajwa. * SCI 1 in combination with any of the following: Rau; Kawamasa; Hasegawa; Saccardi; OR Kumagai.
17[11]	* Saccardi * Yamaguchi * Kumagai * Fischer * Siemens PIP * SCI 1	* Fischer in combination with any of the following: Rau; Kawamasa; Hasegawa; Saccardi; OR Kumagai. * SCI 1 in combination with any of the following: Rau; Kawamasa; Hasegawa; Saccardi; OR Kumagai.
18[17]	* Saccardi * Yamaguchi * Kumagai * Fischer * Siemens PIP * Kanopoulos * Miller * Pelgrom (9/86) * Pelgrom (6/87) * SCI 1	* Fischer in combination with any of the following: Rau; Kawamasa; Hasegawa; Saccardi; OR Kumagai. *Ohno with Rau * SCI 1 in combination with any of the following: Rau; Kawamasa; Hasegawa; Saccardi; OR Kumagai.
19[17]	* Fischer * Siemens PIP SCI 1	* Saccardi in combination with any of the following: Wiggers; Grover; Lofgren; Flora; OR Uvieghara. * Pelgrom (9/86) with Yamaguchi. * Pelgrom (6/87) with Yamaguchi.

7. The '195 Patent Invalidity Contentions		
		* Yamaguchi in combination with any of the following: Wiggers; Grover; Lofgren; Flora; OR Uvieghara. * Kumagai in combination with any of the following: Wiggers; Grover; Lofgren; Flora; OR Uvieghara. * Fischer in combination with any of the following: Rau; Kawamasa; Hasegawa; Saccardi; OR Kumagai, AND in combination with any of the following: Wiggers; Grover; Lofgren; Flora; OR Uvieghara. * SCI 1 in combination with any of the following: Rau; Kawamasa; Hasegawa; Saccardi; OR Kumagai. * Kanopoulos OR Miller OR Ohno with Wiggers; Grover; Lofgren; Flora; OR Uvieghara.

8. The '592 Patent Invalidity Contentions		
Claims	**Anticipated By References**	**Obvious In View Of Reference Combinations**
35	* Saccardi * Yamaguchi * Kumagai * Fischer * Siemens PIP * Kanopoulos * Miller * Pelgrom (9/86) * Pelgrom (6/87) * SCI 1	* Fischer in combination with any of the following: Rau; Kawamasa; Hasegawa; Saccardi; OR Kumagai. * Ohno with Rau; Kawamasa; Hasegawa; Saccardi; Kumagai; OR Bajwa. * SCI 1 in combination with any of the following: Rau; Kawamasa; Hasegawa; Saccardi; OR Kumagai.
38[35]	* Siemens PIP * SCI 1	* Saccardi in combination with any of the following: Wiggers; Grover; Lofgren; Flora; OR Uvieghara. * Pelgrom (9/86) with Yamaguchi. * Pelgrom (6/87) with Yamaguchi.

8. The '592 Patent Invalidity Contentions		
		* Yamaguchi in combination with any of the following: Wiggers; Grover; Lofgren; Flora; OR Uvieghara. * Kumagai in combination with any of the following: Wiggers; Grover; Lofgren; Flora; OR Uvieghara. * Fischer in combination with any of the following: Wiggers; Grover; Lofgren; Flora; OR Uvieghara. * Fischer in combination with any of the following: Rau; Kawamasa; Hasegawa; Saccardi; OR Kumagai, AND in combination with any of the following: Wiggers; Grover; Lofgren; Flora; OR Uvieghara. * SCI 1 in combination with any of the following: Rau; Kawamasa; Hasegawa; Saccardi; OR Kumagai.

9. The '152 Patent Invalidity Contentions		
Claims	**Anticipated By References**	**Obvious In View Of Reference Combinations**
12[11]	* Saccardi * Yamaguchi * Kumagai * Fischer * Siemens PIP * Kanopoulos * Miller * Pelgrom (9/86) * Pelgrom (6/87) * SCI 1	* Fischer in combination with any of the following: Rau; Kawamasa; Hasegawa; Saccardi; OR Kumagai. * SCI 1 in combination with any of the following: Rau; Kawamasa; Hasegawa; Saccardi; OR Kumagai. * Ohno in combination with any of the following: Rau; Kawamasa; Hasegawa; Saccardi; Kumagai; OR Bajwa.
14[11]	* Yamaguchi * Kumagai * Fischer * Siemens PIP * Kanopoulos	* Fischer in combination with any of the following: Rau; Kawamasa; Hasegawa; Saccardi; OR Kumagai. * SCI 1 in combination with any of the following: Rau; Kawamasa; Hasegawa; Saccardi; OR

9. The '152 Patent Invalidity Contentions		
	* Miller * Pelgrom (9/86) * Pelgrom (6/87) * SCI 1	Kumagai.
16[11]	* Fischer * Siemens PIP * Pelgrom (9/86) * Pelgrom (6/87) * SCI 1	* Saccardi in combination with any of the following: Wiggers; Grover; Lofgren; Flora; OR Uvieghara. * Yamaguchi in combination with any of the following: Wiggers; Grover; Lofgren; Flora; OR Uvieghara. * Kumagai in combination with any of the following: Wiggers; Grover; Lofgren; Flora; OR Uvieghara. * Fischer in combination with any of the following: Wiggers; Grover; Lofgren; Flora; OR Uvieghara. * Fischer in combination with any of the following: Rau; Kawamasa; Hasegawa; Saccardi; OR Kumagai, AND in combination with any of the following: Wiggers; Grover; Lofgren; Flora; OR Uvieghara. * SCI 1 in combination with any of the following: Rau; Kawamasa; Hasegawa; Saccardi; OR Kumagai. * Kanopoulos OR Miller OR Ohno in combination with any of the following: Wiggers; Grover; Lofgren; Flora; OR Uvieghara.

Hynix also identifies the following additional references in support of its invalidity contentions:

- Each of **Kawamasa, Hasegawa, Taguri,** and **Mattausch** references discloses every element of the following asserted claims:
  '263 - 1, 2, 3, 4
  '195 - 11,17, 18
  '592 - 35
  '152 - 12, and

Each of the references in (1) in combination with one or more of **Grover, Wiggers, Lofgren, Flora, and Masuda** discloses every element of the following asserted claims:
'195 - 19
'592 - 38
'152 - 16, and

- Each of the references in (1) in combination with **Iqbal, Ohno, Ono, and Poon** discloses every element of the following asserted claims:
'365 - 1
'152 - 14

- **Fujitsu 86-87 data book - MB81461-12, -15** starting at page 1-102 discloses every element of the following asserted claims:
'105 - 31, 40
'214 - 15
'918 - 18

- Each of the references in (4) in combination with **Cydra 5** discloses every element of the following asserted claims:
'214 - 18
'918 -24

- **Advanced Micro Devices 86 data book - AM9OC644** starting at page 4-143 discloses every element of the following asserted claims:
'105 - 31, 40
'214 - 15
'918 - 18, and

- Each of the references in (6) in combination [illegible] **ydra 5** discloses every element of the following asserted claims:
'214 - 18
'918 -24

IV. INVALIDITY CLAIM CHARTS—Patent Local Rule 3-3(c)

Pursuant to Patent Local Rule 3-3(c), attached are the following invalidity claim charts. The charts are organized by comparing each primary prior reference against the asserted claims.

Chart Number	Primary Prior Art Reference
1	Siemens PIP
2	SCI 1
3	Fischer
4	Bajwa
5	Yamaguchi
6	Saccardi
7	Kumagai
8	Gigabit Logic
9	Watanabe
10	Redwine
11	Aichelmann
12	Yoshimoto
13	Tam
14	Ohta
15	Chin
16	Penzel
17	Ong
18	Ebbers
19	Kanopoulus
20	Taguchi
21	Miller
22	Novak
23	Ono

Chart Number	Primary Prior Art Reference
24	Pelgrom (9/86)
25	Pelgrom (6/87)
26	Higuchi
27	Ohno
28	Iqbal
29	SCI 2

///

///

///

V. DEFENSES BASED UPON 35 U.S.C. § 112(1) & (2)—Patent Local Rule 3-3(d)

Local Rule 3.3(d) Contentions

A. INVALIDITY UNDER 35 U.S.C. §112(1)

Hynix contends that the following of the representative claims of the patents in suit are invalid for failure to meet the requirements of 35 U.S.C. § 112, paragraph 1:

Local Rule 3.3(d) Contentions '105 patent, claims 34, 35, 40;
'443 patent, claims 1, 3, 6;
'214 patent, claim 26;
'918 patent, claim 33.
'195 patent, claim 19;
'365 patent, claim 1;
'592 patent, claim 38; and
'152 patent, claim 16.

1. Claims 1,3 And 6 of '443 Patent – 35 U.S.C. §112(1) (Written Description)

Claims 1, 3, and 6 of the '443 patent include the following limitations of claim 1 of this patent:

> a first subarray section having a first internal I/O line to access data from a first memory cell location and a second internal I/O line to access data from a second memory cell location, wherein the first and second memory cell locations are in the first subarray section;
>
> a second subarray section having a first internal I/O line to access data from a third memory cell location and a second internal I/O line to access data from a fourth memory cell location, wherein the third and fourth memory cell locations are in the second subarray section;
>
> the multiplexer circuitry couples the first internal I/O line of the first subarray section to an input of the first output driver and couples the first internal I/O line of the second subarray section to an input of the second output driver in response to the clock edge of the first internal clock signal; and
>
> the multiplexer circuitry couples the second internal I/O line of the first subarray section to an input of the first output driver and couples the second internal I/O line of the second subarray section to an input of the second output driver in response to the clock edge of the second internal clock signal.

The specification of the '443 patent discloses "three different techniques to provide the additional internal I/O line required and to supply data to memory cells at this rate." '443 patent, col.

24:3-31, referencing Figs. 10, 15, and 17. None of these three techniques, and no other disclosure of the '443 patent, includes any description or disclosure of the particular arrangement specifically recited in the claims of the '443 patent, or any disclosure of which and how many cells and cell locations are routed to each of at least two output drivers, or the recited operation of the multiplexer in response to first and second internal clock signal edges. Accordingly, claim 1 of the '443 patent, and claims 3 and 6 which are dependent on and incorporate all of the limitations of claim 1, are invalid for failure to comply with the written description requirement of 35 U.S.C. § 112, paragraph 1.

2. Claim 1 Of The '443 Patent – 35 U.S.C. §112(1) (Written Description)

Claims 1 of the '443 patent also recites:

> clock generation circuitry, coupled to the clock receiver circuitry, to generate a first internal clock signal having a clock edge which is synchronized with the external clock signal and to generate a second internal clock signal having a clock edge which is synchronized with the external clock signal;

The specification of the '443 patent does not disclose the generation of any internal clock signals which are "synchronized" with an external clock signal. The only disclosure of internal clock signals (which are used to operate a multiplexer, as also required by the claim) disclosed in the specification of the '443 patent are internal clock signals 73 and 74, which has a clock edge one receiver delay before the midpoint between the edges of two external clock signals. This midpoint is not synchronized to the clockedges of either external clock; therefore, the internal clocks are not synchronized to any external clock. For this reason also, Claim 1 of the '443 patent, and claims 3 and 6 which are dependent on and incorporate all of the limitations of claim 1, are invalid for failure to comply with the written description requirement of 35 U.S.C. § 112, paragraph 1.

3. "Delay Locked Loop" – 35 U.S.C. §112(1) (Written Description)

The following claims each recite a delay locked loop:

'105 patent, claims 34, 35, 40;
'443 patent, claims 1, 3, 6;
'214 patent, claim 26;
'918 patent, claim 33.
'195 patent, claim 19;
'365 patent, claim 1; and

'592 patent, claim 38.

There is no disclosure in the specifications or drawings, as originally filed, of any of the patents in suit of anything that would have been understood by one of skill in the art at the time the invention was made as a "delay locked loop, or even as a "phase locked loop." Neither the term "delay locked loop" nor the term "phase locked loop" was even introduced into the claims of any of the applications for the patents in suit (or related applications) until several years after the original application for the patents in suit was filed, in April, 1990. No similar or analogous terminology was used in the original application for the patents in suit, and none of the applications leading up to the issuance of the patents in suit actually discloses any circuit or feature that would have been understood by one of skill in the art at the time the invention was made as constituting a delay locked loop. Therefore, these claims are invalid as failing to meet the written description requirement of 35 U.S.C. § 112, paragraph 1.

4. "Delay Locked Loop" – 35 U.S.C. §112(1) (Enablement)

(Enablement) The following claims each recite a delay locked loop:

'105 patent, claims 34, 35, 40;
'443 patent, claims 1, 3, 6;
'214 patent, claim 26;
'918 patent, claim 33;
'195 patent, claim 19;
'365 patent, claim 1; and
'592 patent, claim 38.

Even assuming that the applications for the patents in suit disclose a delay locked loop, the disclosures of a delay locked loop in the patents in suit (all of which are substantially the same for the present purposes) are insufficient to meet the requirements of 35 U.S.C. § 112, paragraph 1. Figures 12 and 13 and their attendant description contain only a high level discussion of the objectives to be achieved by the circuit shown in block diagram in Figure 12. No detail of the circuitry proposed to be included in any of the delay line blocks shown in Figure 12 is disclosed. No instructions or descriptions are provided as to how to design or operate the circuits represented by blocks in Figure 12, including the blocks designated "filter" and delay lines 103, 104, 105, and 106. Given the level of

difficulty, at the time the original application was filed (April, 1990), of designing operable phase- or delay- locked loops, particularly that could operate in connection with the bus clock frequencies disclosed by the inventors (250 MHz), the disclosure in insufficient to enable one of ordinary skill at the time the invention was made to make and use the invention claimed in the above claims without undue experimentation.

B. INVALIDITY DEFENSES UNDER 35 U.S.C. §112(2)

Hynix contends that the following of the representative claims of the patents in suit are invalid for failure to comply with the requirements of 35 U.S.C. § 112, paragraph 2:

'214 patent, claim 18;
'105 patent, claim 35; and
'195 patent, claim 19.

1. Claim 18 of The '214 Patent – 35 U.S.C. §112(2

Claim 18 of the '214 patent, and particularly the term

> "the code being representative of a number of clock cycles of the first and second external clock signals to transpire before data is output onto the bus in response to the first read request,"

is indefinite. It is unclear whether the number of clock cycles of the first and second clocks indicated by the code run concurrently, sequentially, or in some other relationship before data is output. The time after which data is output is thus undefined in any case in which the first and second external clocks have different frequencies or phases or both. Claim 18 is thus invalid for failing to particularly point out and distinctly claim any subject matter regarded as an invention.

2. Claim 35 Of The '105 Patent – 35 U.S.C. §112(2)

Claim 35 of the '105 patent contains no antecedent basis for the term "first and second internal clock generation circuitry." The other portions of the claim, and the claims on which claim 35 are dependent refer only to "internal clock generation circuitry" and include no reference to "first and second clock generation circuitry. Claim 35 is thus invalid for failing to particularly point out and

distinctly claim any subject matter regarded as an invention.

3. Claim 19 Of The '105 Patent – 35 U.S.C. §112(2)

Claim 19 of the '105 patent refers to "the plurality of output drivers." The other portions of this claim and the claims upon which claim 19 is dependent make no reference to either output drivers or a plurality of output drivers. Claim 19 is thus invalid for failing to particularly point out and distinctly claim any subject matter regarded as an invention.

C. INVALIDITY BASED UPON RAMBUS' CLAIM CONSTRUCTION – 35 U.S.C. §112(1)

In addition, Hynix contends that, if certain terms in the representative claims of the patents in suit are construed as apparently contended by Rambus, then the following of the representative claims are invalid for failure to meet the written description requirement of 35 U.S.C. § 112, paragraph 1:

'105 patent, claims 31, 34, 35, 40;
'263 patent, claims 1, 2, 3, 4;
'443 patent, claims 1, 3, 6;
'214 patent, claims 15, 18, 25, 26;
'918 patent, claims 18, 24, 33.;
'195 patent, claims 11, 17, 18, 19;
'365 patent, claims 1, 4; and
'592 patent, claims 35, 38.
'152 patent, claims 12, 14, 16;

The basis of these contentions is outlined below.

1. "Bus" – 35 U.S.C. §112(1)

Rambus appears to construe the term "bus" as "a plurality of signal lines between two electrically communicating devices" or another similarly broad construction. If the term "bus" is interpreted in this or a similar manner, at least the following representative claims of the patents in suit are invalid for failure to meet the written description requirement of 35 U.S.C. § 112, paragraph 1:

'105 patent, claims 31, 34, 35, 40;
'263 patent, claims 2, 3;
'443 patent, claims 1, 3, 6;
'214 patent, claims 15, 18, 25, 26;
'918 patent, claims 18, 24, 33;

'195 patent, claims 11, 17, 18, 19;
'365 patent, claims 1, 4; and
'592 patent, claims 35, 38.

The specifications of the patents in suit, which are substantially identical for the purposes of these contentions, expressly limit the type and characteristics of the bus recited in these claims. The following are exemplary statements from the specifications of the patents in suit expressing such limitations (column and line references are to the specification of the '152 patent; the corresponding references to the specifications of the other patents in suit vary slightly):

> **The present invention includes a memory subsystem comprising at least two semiconductor devices, including at least one memory device, connected in parallel to a bus, where the bus includes a plurality of bus lines for carrying substantially all address, data and control information needed by said memory devices,** where the control information includes device-select information and the bus has substantially fewer bus lines than the number of bits in a single address, and the bus carries device-select information without the need for separate device-select lines connected directly to individual devices. ['152; 3:44-54]
>
> * * *
>
> Referring to FIG. 2, a standard DRAM 13, 14, ROM (or SRAM) 12, microprocessor CPU 11, I/O device, disk controller or other special purpose device such as a high speed switch is modified to **use a wholly bus-based interface rather than the prior art combination of point-to-point and bus-based wiring used with conventional versions of these devices. The new bus includes clock signals, power and multiplexed address, data and control signals.** In a preferred implementation, 8 bus data lines and an AddressValid bus line carry address, data and control information for memory addresses up to 40 bits wide. Persons skilled in the art will recognize that 16 bus data lines or other numbers of bus data lines can be used to implement the teaching of this invention. **The new bus is used to connect elements such as memory, peripheral, switch and processing units.** ['152, col. 3:55 – 4:3]
>
> **In the system of this invention, DRAMs and other devices receive address and control information over the bus and transmit or receive requested data over the same bus.** Each memory device contains only a single bus interface with no other signal pins. ['152; 4:3-8]
>
> * *

The present invention is designed to provide a high speed, multiplexed bus for communication between processing devices and memory devices and to provide devices adapted for use in the bus system. The invention can also be used to connect processing devices and other devices, such as I/O interfaces or disk controllers, with or without memory devices on the bus. **The bus consists of a relatively small number of lines connected in parallel to each device on the bus. The bus carries substantially all address, data and control information needed by devices for communication with other devices on the bus.** In many systems using the present invention, the bus carries almost every signal between every device in the entire system. There is no need for separate device-select lines since device-select information for each device on the bus is carried over the bus. There is no need for separate address and data lines because address and data information can be sent over the same lines. ['152; 5:24-40]

* * *

All information sent between master devices and slave devices is sent over the external bus, which, for example, may be 8 bits wide. This is accomplished by defining a protocol whereby a master device, such as a microprocessor, seizes exclusive control of the external bus (i.e., becomes the bus master) and initiates a bus transaction by sending a request packet (a sequence of bytes comprising address and control information) to one or more slave devices on the bus. An address can consist of 16 to 40 or more bits according to the teachings of this invention. Each slave on the bus must decode the request packet to see if that slave needs to respond to the packet. ['152; 6:47-58]

* * *

In the **bus-based system of this invention,** a mechanism is provided to give each device on the bus a unique device identifier (device ID) after power-up or under other conditions as desired or needed by the system. A master can then use this device ID to access a specific device, particularly to set or modify registers 170 of the specified device, including the control and address registers. In the preferred embodiment, ... ['152; 14:44-51]

* * *

The **bus architecture of this invention** makes possible an innovative 3-D packaging technology. By using a **narrow, multiplexed (time-shared) bus,** the pin count for an arbitrarily large memory device can be kept quite small--on the order of 20 pins. Moreover, this pin count can be kept constant from one generation of DRAM density to the next. ['152: 17:23-28]

> The method of this invention does not require changing the overall method used for column access, but does change implementation details. Many of these details have been implemented selectively in certain fast memory devices, but **never in conjunction with the bus architecture of this invention.** ['152; 23:57-62]

The stated objects of the invention are in full accord with these limiting statements, as is the characterization of the prior art contained in the specifications of all of the patents in suit.

The '152 patent, and all of the patents in suit, clearly describe the invention as limited to a system, method, or device(s) incorporating, operable with, or interfacing to only a narrow bus with a multiplexed set of signal lines used to transmit address, data, and control information. In view of the disclosure of each of the patents in suit, one of skill in the art would understand the specification accordingly. To the extent the term "bus" is interpreted more broadly, the above claims are invalid for failure to comply with the written description requirement of 35 U.S.C. § 112, paragraph 1.

2. The Term "Synchronized Memory Device" – 35 U.S.C. §112(1)

Rambus appears to construe the term "synchronous memory device" as "a memory device in which address, data, and control signals are recognized and/or transferred in response to an external clock" or another similar definition. If the term "synchronous memory device" is interpreted in this or a similar manner, at least the following representative claims of the patents in suit are invalid for failure to meet the written description requirement of 35 U.S.C. § 112, paragraph 1:

'105 patent, claims 31, 34, 35, 40;
'152 patent, claims 12, 14, 16;
'195 patent, claims 11, 17, 18, 19;
'214 patent, claims 15, 18, 25, 26;
'263 patent, claims 1 - 4;
'365 patent, claims 1, 4;
'443 patent, claims 1, 3, 6;
'592 patent, claims 35, 38; and
'918 patent, claims 18, 24, 33.

The specifications of the patents in suit, which are substantially identical for the purposes of these contentions, expressly limit the type and characteristics of the "synchronous memory device" recited in these claims. The following are exemplary statements from the specifications of the patents

in suit expressing such limitations (column and line references are to the specification of the '152 patent; the corresponding references to the specifications of the other patents in suit vary slightly):

> **The present invention includes a memory subsystem comprising at least two semiconductor devices, including at least one memory device, connected in parallel to a bus, where the bus includes a plurality of bus lines for carrying substantially all address, data and control information needed by said memory devices,** where the control information includes device-select information and the bus has substantially fewer bus lines than the number of bits in a single address, and the bus carries device-select information without the need for separate device-select lines connected directly to individual devices. ['152; 3:44-54]
>
> * * *
>
> **In the system of this invention, DRAMs and other devices receive address and control information over the bus and transmit or receive requested data over the same bus. Each memory device contains only a single bus interface with no other signal pins.** ['152; 4:3-8]
>
> * * *
>
> **The present invention is designed to provide a high speed, multiplexed bus for communication between processing devices and memory devices and to provide devices adapted for use in the bus system.** The invention can also be used to connect processing devices and other devices, such as I/O interfaces or disk controllers, with or without memory devices on the bus. **The bus consists of a relatively small number of lines connected in parallel to each device on the bus.** The bus carries substantially all address, data and control information needed by devices for communication with other devices on the bus. In many systems using the present invention, the bus carries almost every signal between every device in the entire system. There is no need for separate device-select lines since device-select information for each device on the bus is carried over the bus. There is no need for separate address and data lines because address and data information can be sent over the same lines. ['152; 5:24-40]
>
> * * *
>
> All information sent between master devices and slave devices is sent over the external bus, which, for example, may be 8 bits wide. This is accomplished by defining a protocol whereby a master device, such as a microprocessor, seizes exclusive control of the external bus (i.e., becomes the bus master) and initiates a bus transaction by sending a request packet (a sequence of bytes comprising address and control

> information) to one or more slave devices on the bus. An address can consist of 16 to 40 or more bits according to the teachings of this invention. Each slave on the bus must decode the request packet to see if that slave needs to respond to the packet. ['152; 6:47-58]
>
> * * *
>
> In the **bus-based system of this invention, a mechanism is provided to give each device on the bus** a unique device identifier (device ID) after power-up or under other conditions as desired or needed by the system. A master can then use this device ID to access a specific device, particularly to set or modify registers 170 of the specified device, including the control and address registers. In the preferred embodiment, ... ['152; 14:44-51]

The stated objects of the invention are in full accord with these limiting statements, as is the characterization of the prior art contained in the specifications of all of the patents in suit.

The '152 patent, and all of the patents in suit, clearly describe the invention as limited to a system, method, or device(s) incorporating, operable with, or interfacing to only a narrow bus with a multiplexed set of signal lines used to transmit address, data, and control information. In view of the disclosure of each of the patents in suit, one of skill in the art would understand the specification accordingly, and understand that a "synchronous memory device" is limited to a memory device with an interface to the narrow, multiplexed bus disclosed in the specifications. To the extent the term "synchronous memory device" is interpreted more broadly, the above claims are invalid for failure to comply with the written description requirement of 35 U.S.C. § 112, paragraph 1.

3. "Read Request" – 35 U.S.C. §112(1)

Rambus appears to construe the term "read request" as "a message, instruction, or command received by a memory device directing, instructing, or commanding the memory device to output data" or another similar definition, without regard to whether the message, instruction of command occurs over a plurality of clock cycles or whether it provides a sufficient address to allow the memory device to unambiguously determine which data are to be read out in response. If the term "read request" is interpreted in this or a similar manner, at least the following representative claims of the patents in suit are invalid for failure to meet the written description requirement of 35 U.S.C. § 112, paragraph 1:

'263 patent, claims 1, 2, 3, 4;
'443 patent, claims 1, 3, 6;
'214 patent, claims 15, 18, 25, 26;
'918 patent, claims 18, 24, 33;
'195 patent, claims 11, 17, 18, 19;
'365 patent, claims 1, 4; and
'592 patent, claims 35, 38.

All embodiments (actually, the single embodiment) disclosed in the patents in suit (all of which have the same disclosure for present purposes) utilize "request packets" to both transmit instructions or commands (and data, for memory array write operations) to a memory device and receive responses from the memory device. The use of such packets is crucial to the operation of the disclosed narrow, multiplexed bus and the attainment of the stated advantages of systems constructed using this bus. Even assuming that a read request need not necessarily take the form of a packet per se, one of ordinary skill would recognize from these and other aspects of the disclosure of the patents in suit that, at a minimum, a read request must include control information designating at least the type of operation to be performed and sufficient address information to allow a memory device to respond to the request by reading out unambiguously specified data. One of ordinary skill would also recognize from the disclosure that the read request must be transmitted over the narrow, multiplexed bus of the invention over multiple clock cycles in order to attain the stated advantages and objective of the disclosed embodiment. To the extent that the above claims are or can be interpreted more broadly than this, the above claims are all invalid for failure to satisfy the written description requirement of 35 U.S.C. § 112, paragraph 1.

4. "External Clocks" – 35 U.S.C. §112(1)

Rambus appears to construe the each of the terms "first external clock" and "second external clock" as a clock signal external to the memory device" or another similar definition. If the terms "first external clock" and "second external clock" are interpreted in this or a similar manner, at least the following representative claims of the patents in suit are invalid for failure to meet the written description requirement of 35 U.S.C. § 112, paragraph 1:

'105 patent, claim 40;
'214 patent, claims 15, 18, 25, 26;
'365 patent, claims 1, 4; and
'152 patent, claim 14.

The Rambus patents in suit, all of which have substantially the same specification for present purposes, disclose only one clocking scheme, in which a single clock signal is routed to each device on the bus twice – on an outgoing path and a return path. Each device on the bus samples the clock signal on both paths; these two samplings are the only clock signals disclosed that could be considered first and second external clocks. Due to flight time delays, the clock signals sampled each individual device are out of phase, the mid-point between the edges of the two sampled clock signals occur at the same time for all devices on the bus. In this way, each device determines the "system" clock, which is the same for all devices on the bus. The use of this "system" clock signal, represented by the mid-points of the early and late clock signals is crucial to the proper operation all disclosed or suggested variants of the single disclosed embodiment of the invention. One of ordinary skill would understand that this disclosed clocking system requires that the first and second external clock signals each individually provide different timing information to any particular device, such that a common "system" clock can be determined. To the extent that the above claims are or can be interpreted not to require that the first and second clocks each provide different timing information to any particular device, the above claims are invalid for failure to satisfy the written description requirements of 35 U.S.C. § 112, paragraph 1.

///

///

///

VI. DOCUMENT PRODUCTION—Patent Local Rule 3-4

In accord with Patent Local Rule 3-4(a), Hynix previously produced technical documents sufficient to show the operation of the accused Hynix products.

In accord with Patent Local Rule 3-4(b), Hynix has previously produced most of the prior art references identified by Hynix pursuant to Patent Local Rule 3-3(a). The bates numbers for the previously produced documents are identified in Exhibit A. Hynix is also doing copies of the following references:

Exhibit	Prior Art Reference
B	Referenced Document Chart
C	1986-87 Data Book Memories (Fujitsu)
D	1986 Bipolar/MOS Memories Data Book (Advanced Micro Devices)
E	1987 "A-32-kbit Variable-Length Shift Register for Digital Audio Application," Marcel J.M. Pelgrom, et al.

DATED: October 1, 2001

Respectfully submitted,

By: _____
Jordan Trent Jones

Daniel J. Furniss (State Bar No. 73531)
Theodore G. Brown, III (State Bar No. 114672)
Jordan Trent Jones (State Bar No. 166600)
TOWNSEND AND TOWNSEND AND CREW LLP
379 Lytton Avenue
Palo Alto, California 94301
Telephone: (650) 326-2400
Facsimile: (650) 326-2422

Attorneys for
HYNIX SEMICONDUCTOR INC.,
HYNIX SEMICONDUCTOR AMERICA, INC.,
HYNIX SEMICONDUCTOR U.K. LTD., and
HYNIX SEMICONDUCTOR DEUTSCHLAND GmbH

PA 3173375 v8

TABLE OF CONTENTS

TAB NO.		
A		Referenced Documents Chart
	1	Siemens PIP
	2	SCI 1
	3	Fischer
	4	Bajwa
	5	Yamaguchi
	6	Saccardi
	7	Kumagai
	8	Gigabit Logic
	9	Watanabe
	10	Redwine
	11	Aichelmann
	12	Yoshimoto
	13	Tam
	14	Ohta
	15	Chin
	16	Penzel
	17	Ong
	18	Ebbers
	19	Kanupoulus
	20	Taguchi
	21	Miller
	22	Novak

TAB NO.

23	Ono
24	Pelgrom (9/86)
25	Pelgrom (6/87)
26	Higuchi
27	Ohno
28	Iqbal
29	SCI 2
B	1986-87 Data Book Memories (Fujitsu)
C	1986 Bipolar/MOS Memories Data Book (Advanced Micro Devices)
D	1987 "A 32-kbit Variable-Length Shift Re[illegible]igital Audio Application," Marcel J.M. Pelgrom, et al.

October 1, 2001

PROOF OF SERVICE

I hereby certify and declare under penalty of perjury that the following statements are true and correct:

1. I am over the age of 18 years and am not a party to the within cause. My business address is 379 Lytton Avenue, Palo Alto, California 94301.

2. Following said practice, on October 1, 2001, I caused to be served by express courier a true copy of the attached document titled exactly **HYNIX' PRELIMINARY INVALIDITY CONTENTIONS** to the following:

Cecilia H. Gonzalez
Joseph P. Lavelle
Basil C. Culyba
HOWREY SIMON ARNOLD & WHITE, LLP
1299 Pennsylvania Avenue, N.W.
Washington, D.C. 20004

Evangelina M. Almirantearena
HOWREY SIMON ARNOLD & WHITE, LLP
301 Ravenswood Avenue
Menlo Park, CA 94025

EXECUTED this 1st day of October, 2001, at Palo Alto, California.

Mary Bernstein

EXHIBIT A

REFERENCED DOCUMENTS

C'try of Origin / Patent No.	Inventor	Date of Issue	Referenced As	Title	Begin Bates	End Bates
US 4,998,262	Hans A.M. Wiggers	03/05/1991	Wiggers (US262)	Generation Of Topology Independent Reference Signals	HR905_010509	HR905_010515
US 5,184,027	Masuda, Norboru; Kamikawai, Ryotaro; Yagyu, Masayoshi; Yamamoto, Masakazu	02/02/1993	Masuda	Clock Signal Supply System	HR905_010647	HR905_010705
US 4,870,562	Kimoto, Manabu; Nishiguchi, Yukihiro	09/26/1989		Microcomputer Capable Of Accessing Internal Memory At A Desired Variable Access Time	HR905_010756	HR905_010769
US 4,754,433	Daeje Chin; Wei Hwang; Nicky C. Lu	06/28/1988	Chin	Dynamic Ram Having Multiplexed Twin I/O Line Pairs	HR905_010859	HR905_010867
US 4,726,021	Aoki, Masakazu	02/16/1988		Semiconductor Memory Having Error Correcting Means	HR905_010883	HR905_010913
US 5,001,672	Timothy J. Ebbers; Satish Gupta; Randall L. Henderson; Nathan R. Hiltebeitel; Robert Tamlya; Steven W. Tomashot; Todd Williams	03/19/1991	Ebbers (US672)	Video RAM with External Select of Active Serial Access Register	HR905_010934	HR905_010943
US 4,928,265	Higuchi, Hisayuki; Homma, Noriyuki; Suzuki, Makota; Tachibana, Suguru	05/22/1990	Higuchi	Semiconductor Integrated Circuit	HR905_010970	HR905_010990
US 4,849,937	Masahiko Yoshimoto	07/18/1989	Yoshimoto (US937)	Digital Delay Unit with Interleaved Memory	HR905_010991	HR905_011004
US 4,330,852	Donald J. Redwine; Lionel S. White, Jr.; G.R. Mohan Rao	05/18/1982	Redwine	Semiconductor Read/Write Memory Array Having Serial Access	HR905_011345	HR905_011354
JP 64-29951	Takashi Kumagai	01/31/1989	Kumagai (JP951)	Storage System (translation included)	HR905_011487	HR905_011498
JP 61-72350	Hashimoto, Shigeru; Nishimura, Naoyuki	04/14/1986		Data Transfer Control System (translation included)	HR905_011499	HR905_011514

REFERENCED DOCUMENTS

C'try of Origin / Patent No.	Inventor	Date of Issue	Referenced As	Title	Begin Bates	End Bates
JP 63-142445	Yasushi Taguchi; Hiroshi Murata	06/14/1988	Taguchi	Memory Device	HR905_011515	HR905_011532
JP 60-80193	Jun Hasegawa; Kazuhiko Honma	05/08/1985		Memory System (translation included)	HR905_011533	HR905_011544
JP 56-82961	Kunihiro Kawamasa	07/07/1981		Memory Control Method (translation included)	HR905_011545	HR905_011554
JP 57-14922	Junichi Taguri	01/26/1982		Memory Storage Device (translation included)	HR905_011577	HR905_011584
US 4,628,489	Richard H. Ong; Peter C. Enconomopoulos; Russel W. Guenthner	12/09/1986	Ong (US489)	Dual Address RAM	HR905_011665	HR905_011682
US 4,680,738	Tam, Aloysuis T.	07/14/1987	Tam	Memory With Sequential Mode	HR905_011841	HR905_011849
US 4,631,659	John Hayne, II; John Schabowski	12/23/1986		Memory Interface With Automatic Delay State	HR905_011878	HR905_011917
US 4,785,394	Fischer, Michael A.	11/15/1988	Fischer	Fair Arbitration Technique for a Split Transaction Bus in a Multiprocessor Computer System	HR905_021423	HR905_021466
US 4,562,435	McDonough, Kevin C; Hughes, John M; Laffitte, David	12/31/1985		Video Display System Using Serial/Parallel Access Memories	HR905_022539	HR905_022558
US 5,361,277	Wayne D. Grover	11/01/1994	Grover (US277)	Method And Apparatus For Clock Distribution And For Distributed Clock Synchronization	HR905_023452	HR905_023479
US 4,360,870	McVey, James	11/23/1982		Programmable I/O Device Identification	HR905_023821	HR905_023828
JP 63-217452	Saito Takashi	09/09/1988		Setting System for Memory Access Timing	HR905_024236	HR905_024244
US 4,499,536	Gemma, Kazutoshi; Ishibashi, Michiyasu	02/12/1985		Signal Transfer Timing Control Using Stored Data Relating to Operating Speeds of Memory and Processor	HR905_024498	HR905_024507
US 4,663,735	Mark F. Novak; Karl M. Guttag	05/05/1987	Novak	Random/Serial Access Mode Selection Circuit For A Video Memory System	HR905_024508	HR905_024525
US 4,845,664	Frederick J. Aichelmann, Jr.; Bruce E. Bachman	06/04/1989	Aichelmann (US664)	On-Chip Bit Reordering Structure	HR905_024549	HR905_024560

REFERENCED DOCUMENTS

C'try of Origin / Patent No.	Inventor	Date of Issue	Referenced As	Title	Begin Bates	End Bates
US 4,536,795	Hirota, Akira; Miyahara, Hiroyuki; Kosaka, Yohiteru	08/20/1985		Video Memory Device	HR905_024664	HR905_024678
US 4,825,287	Baji, Toru; Matsuura, Tasuji; Tsukada, Toshiro; Ohba, Shinya	04/25/1989		Digital Video Signal Processor	HR905_024679	HR905_024701
US 4,637,018	Laurence P. Flora; Michael A. McCullough	01/13/1987	Flora (US018)	Automatic Signal Delay Adjustment Method	HR905_024971	HR905_024979
JP 64-43894	Ono, Naoya	02/16/1989	Ono (JP894)	Semiconductor Memory (translation included)	HR905_024980	HR905_024993
GB 02197553A	Lofgren, K.M. et al.	05/18/1988	Lofgren (GB553A)	Phase-locked Loop Delay Line	HR905_025015	HR905_025028
US 4,763,249	Bomba, Frank C.; Reinhard Schumann; Stephen R. Jenkins; Paul Binder	08/09/1988		Bus Device For Use In A Computer System Having A Synchronous Bus	HR905_025072	HR905_025119
US 5,006,982	Ronald J. Ebersole; David Johnson; David Budde; Mark S. Myers; Gerhard Bier	04/09/1991		Method of Increasing the Bandwidth of a Packet Bus by Reordering Reply Packets	HR905_025176	HR905_025191
US 4,394,753	Penzel, Hangs-Joerg	07/19/1983	Penzel	Integrated Memory Module Having Selectable Operating Functions	HR905_025235	HR905_025252
US 4,858,113	Raymond J. Saccardi	08/15/1989	Saccardi (US113)	Reconfigurable Pipelined Processor	HR905_025281	HR905_025289
US 4,785,428	Atiq Bajwa; Robert Duzett; M. Vittal Kini; Kent Mason; Mark S. Myers; Sunil Shenoy	11/15/1988	Bajwa	Programmable Memory Array Control Signals	HR905_025303	HR905_025314
JP 63-239676	Yamaguchi, Yasunori	10/05/1988	Yamaguchi (JP676)	Semiconductor Memory Device	HR905_026225	HR905_026238
JP 63-239676				Translation	HR905_032533	HR905_032562
US 4,688,197	Mark F. Novak et al.	08/18/1987	Novak	Control Of Data Access To Memory For Improved Video System	HR905_065539	HR905_065557

REFERENCED DOCUMENTS

C'try of Origin / Patent No.	Inventor	Date of Issue	Referenced As	Title	Begin Bates	End Bates
JP 63-46864	Junichi Taguri	09/19/1988		Memory Storage Device (translation included)	HR905_066561	HR905_066564
JP 63-217452				Translation	HR905_105708	HR905_105717
US 4,789,960	Willis, Donald H.	12/06/1988		Dual Port Video Memory System Having A Semi-Synchronous Data Input And Data Output	HR905_105718	HR905_105731
US 4,597,019	Nishimoto, Naomichi; Yutaka Ichinoi	06/24/1986		Clock Pulse Generating Circuit In A Color Video Signal Reproducing Apparatus	HR905_105741	HR905_105757
US 5,099,481	Miller, Michael J.	05/24/1992	Miller	Registered Ram Array With Parallel And Serial Interface	HR905_105758	HR905_105770
US 4,755,937	Glier, Michael T.	07/05/1988		Method And Apparatus For High Bandwidth Shared Memory	HR905_105851	HR905_105857
Author	**Publication**	**Date**	**Referenced As**	**Title**	**Begin Bates**	**End Bates**
		08/00/1989	Siemens PIP	Siemens P-I-P System - IC's For Entertainment (Includes Device Data Sheets)	HR905_024199	HR905_024235
Ramakrishna B. Rau	IEEE	01/06/1989	Rau (Cydra 5)	The Cydra-5 Departmental Supercomputer Design Philosophies, Decisions, and Trade-offs	HR905_067546	HR905_067567
Schanke, Morten		05/05/1989	SCI-B [used re SCI 1 and SCI 2]	Proposal for Clock Distribution in SCI	HR905_105320	HR905_105324
		11/00/1988		Norsk Data Report	HR905_105838	HR905_105850
		11/00/1988		P1596: SCI, A Scalable Coherent Interface Bus Specification Components	HR905_105809	HR905_105832
Gustavson, David B. et al		08/22/1988	SCI-A [used re SCI 1 and SCI 2]	The Scalable Coherent Interface Project (Superbus)	HR905_105784	HR905_105808
Gustavson, David B.		11/28/1988	SCI-C [used re SCI 1 and SCI 2]	Scalable Coherent Interface	HR905_105286	HR905_105310
James, David V.		11/28/1988		Scalable I/O Architecture for Buses	HR905_105314	HR905_105319

REFERENCED DOCUMENTS

Author	Publication	Date	Referenced As	Title	Begin Bates	End Bates
S. Watanabe et. al.	IEEE Journal of Solid State Circuits, vol. 24 No. 4, pp. 900-904	08/00/1989	Watanabe – ISSCC '89	An Experimental 16-Mbit CMOS DRAM Chip with a 100-MHz Serial Read/Write Mode	HR905_010388	HR905_010396
Gregory Uvieghara et al	IEEE Journal of Solid-State Circuits, vol. 25, No. 1, pp. 84-89	02/00/1990	Uvieghara (JSSCC, 2/90)	An On-Chip Smart Memory for a Data-Flow CPU	HR905_024312	HR905_024322
Hans-Jürgen Mattausch et al.	IEEE Journal of Solid-State Circuits, vol. 23, no. 1, pp. 105-110	02/00/1988		A Memory-Based High-Speed Digital Delay Line with a Large Adjustable Length	HR905_024275	HR905_024280
Kanopoulos, Nick and Jill J. Hallenbeck	IEEE Transactions on Circuits and Systems, Vol. CAS-33, No. 5, pp. 556-558	05/00/1986	Kanopoulos	A First-In, First-Out Memory for Signal Processing Applications	HR905_065589	HR905_065591
K. Ohta	IEEE Journal of Solid State Circuits, vol. 21 No. 5, pp. 649-654	10/00/1986	Ohta – JSSCC 10/86	A 1-Mbit DRAM with 33-MHz Serial I/O Ports	HR905_010381	HR905_010387
Schnaitter, William M. et al.	IEEE Journal of Solid-State Circuits, vol. SC-21, no. 5, pp. 720-726	10/00/1986		A 0.5-GHz CMOS Digital RF Memory Chip	HR905_010441	HR905_010447
M. Pelgrom et al.	ESSCIRC Dig. Tech. Papers, pp.38-40	09/00/1986	Pelgrom 9/86	A 32Kbit Variable Length Shift Register for Digital Audio Application	HR905_032563	HR905_032565
Gigabit Logic Inc.		08/00/1989	Gigabit Logic	1989 GaAs IC Data Book & Designer's Guide	HR905_024108	HR905_024192
K. Numata et. al.	IEEE Journal of Solid State Circuits, vol. 24 No. 4, pp. 900-904	08/00/1989		New Nibbled -Page Architecture for High Density DRAM's	HR905_010375	HR905_010380
Bursky, Dave	Electronic Design, pp. 145-147	02/22/1990		Advanced Self-Timed SRAM Pares Access Time to 5 ns	HR905_010435	HR905_010440
Ohno, Chikai	Fujitsu Sci. Tech. J., Vol. 24, No. 4, pp. 293-300	12/00/1998	Ohno	Self-Timed ram: STRAM	HR905_010333	HR905_010343

REFERENCED DOCUMENTS

Author	Publication	Date	Referenced As	Title	Begin Bates	End Bates
Poon, TC, et al.	IEEE Journal of Solid State Circuits, Vol. SC-22, No. 3, pp. 491-494	00/00/1987	Poon	A CMOS DRAM-Controller Chip Implementation	HR905_019406	HR905_019410
Iqbal, Mohammad Shakaib	Electronic Design, pp. 93-96	08/25/1988		Internally Timed RAMs Build Fast Writable Control Stores	HR905_010486	HR905_010490
Fujitsu		1986-87		Data Book Memories	HR905_105858	HR905_105886
Advanced Micro Devices		1986		Bipolar/MOS Memories Data Book	HR905_105887	HR905_105909
M. Pelgrom et al.	IEEE Journal of Solid-State Circuits, Vol. SC-22, No. 3, pp. 415-422	06/00/1987	Pelgrom 6/87	A 32-kbit Variable-Length Shift Register for Digital Audio Application	HR905_106285	HR905_106292
Graham, Andy; Sando, Stewart; Gigabit Logic Inc.	Electric Design, pp. 157-170	12/27/1984		Pipelined Static RAM Endows Cache Memories With 1-ns Speed	HR905_010420	HR905_010429